III. Remarks

Acceptance and favorable action therefor of the present application in view of this responsive amendment is respectfully requested.

The status of the claims now pending are given hereinabove. Namely, claims 1, 2, 4, 5, 7, 10, 12, 14-18, 21, 23, 24 and 26 are currently being amended and claims 28 and 29 are being canceled but, however, without prejudice or disclaimer thereof. Claim 22 was previously withdrawn due to an earlier election requirement.

Amendments were made to the claims in consideration of obviating each and every previously outstanding objection directed thereto as well as any and all questions of definiteness of the outstanding Office Action. Also, additional changes were effected in the claims to further clarify the subject matter sought to be covered therein including in a manner which is defining over the art documents cited in the outstanding art rejections. Accordingly, insofar as presently applicable, the previously standing objection of the claims, as detailed under item 5, on page 3 of the Office Action, as well as the rejection under 35 USC §112, second paragraph, are traversed and reconsideration and withdrawal of the same is respectfully requested. That is, each of the previously standing concerns were addressed in connection with the amendments presently made. For example, expressions such as "to be" are no longer present in the claims. Moreover, each of the previously standing concerns under items 8 - 16 on pages 3-4 of the Office Action were further clarified and/or those claims were further defined.

With regard to independent claim 1, the semiconductor module features a stress relaxing layer in connection with the "insulating resin layer." The insulating resin layer is defined as having a thickness greater than the semiconductor device and also functions to relax stress between the semiconductor module and a board

to which the module is mounted. With regard to Fig. 1 of the drawings, as an example thereof, low elastic modulus layer 10, which is frame-shaped, acts as a stress compliant layer. Independent claim 4 similarly features an "insulating resin layer" which acts as a stress relaxing layer and has both an inclined portion as well as a flat portion, the latter on which the external connection terminal (e.g., 5 in Fig. 1) is arranged. Also according to independent claim 2, a part of the wiring that is electrically connected between a terminal on the semiconductor device and the external connection terminal is formed on the inclined portion of the insulating resin layer. This can be seen in Fig. 1 of the drawings which shows wiring connections between the external connection terminal 5 on the flat surface of the insulating resin layer 10 and the terminals 6 on the semiconductor device 1, which wiring is extended over the inclined portion of the insulating resin layer 10 (see Fig. 8F which shows an example of the formation of wires 3 over the inclined plane surface).

Independent claim 4 also calls for a stress relax layer as well as the collective formation, such as, by printing with a mask on a board the plurality of insulating resin layers of the types such as shown in connection with Fig. 1 of the drawings. Figs. 10A and 10B show a mask opening scheme in connection with the formation of the insulating resin layer. Fig. 35 shows one example of the collective printing of plural insulating layers using a mask process.

Independent claim 15 calls for a scheme which, among other featured aspects thereof, the semiconductor module connects a semiconductor device (e.g., chip) and a wiring substrate which are connected via a semiconductor device bump and which does not require an underfill. However, the semiconductor module according to claim 15, likewise, calls for a stress relax layer and also calls for a silicon substrate. An example of this is shown in connection with Fig. 30 of the drawings, although not limited thereto. In independent claim 16, the connection

between the device (chip) and the wiring substrate is effected without the need of an underfill. The invention therein also calls for a semiconductor layer that includes a stress relaxing layer, the stress relaxing layer being associated with the semiconductor device.

With regard to independent claim 17, moreover, the semiconductor module includes a "first stress relaxing layer" that is formed on a side of the wiring substrate to which the semiconductor device is mounted and also calls for the semiconductor device to include a "second insulating resin layer" which functions as a stress relaxing layer between that of the chip and the wiring substrate. Fig. 30, etc., although not limited thereto, is an example of a semiconductor module that may contain such featured aspects. It is submitted, the invention as called for in the above discussed claims as well as in connection with all other ones of the presently pending claims is a patentable improvement over that previously known and, moreover, could not have been attainable from even the combined teachings of the references, as applied in the respective outstanding rejections.

According to the outstanding Office Action, all rejection to the claims were made insofar as those claims where definite, according to the Examiner. Namely, claims 1, 2, 5-8, 10-14, 24, 26 and 27 were rejected under 35 USC §103(a) over the combination of Launay (US 6,320,753) in view of Yukawa (US 6,436,733); claims 3 and 4 also were rejected under 35 USC §103(a) over that same combination of Launay and Yukawa and further in view of Shoji (US 6,054,171); claim 9 was rejected under 35 USC §103(a) over the combination of Launay and Yukawa, as applied to claim 1, and further in view of Hembree (US 6,242,932); claims 15-19, 21 and 25 were rejected under 35 USC §103(a) over the combination of Launay and Yukawa, as applied to claims 1 and 2, and further in view of Lee (US 5,986,334); claim 20 was rejected under 35 USC §103(a) over Launay, Yukawa and Lee, as

applied to claims 1 and 16, and further in view of Shoji (*supra*); and claims 28 and 29 were rejected under 35 USC §103(a) over Launay and Yukawa, as applied to claims 1 and 16, and further in view of the combined teachings of Lee and Shoji (*supra*). It will be shown, hereinbelow, the invention according to claims 1-27, as now amended, could not have been rendered obvious from the combined teachings as alleged in the respective rejections. Accordingly, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

The present invention is directed to a semiconductor module with a high production efficiency in terms of the reliability of its connection to, for example, an external substrate, as well as achieving good reliability in the connections within the module such as between the semiconductor device and the substrate, without the need for an underfill. Such could not have been realizable even in view of the combined teachings of the above-referred to cited art documents.

Launay disclosed a circuit board apparatus and its manufacturing method. Launay's integrated circuit board scheme combines external contact zones and an antenna as well as a process of manufacturing such a board. Specifically, Launay's "invention relates to an integrated circuit board comprising a support, a strip fixed onto the support, a cavity at least partially defined in the support and/or the strip, an integrated circuit provided with connection ends and arranged in the said cavity, an antenna provided with connection terminals and arranged between said support and the said strip, and external contact zones connected to other connection terminals, the said integrated circuit being connected both to the antenna and to the external contact zones, characterized by the fact that the ... connection terminals are arranged opposite corresponding connection ends of the integrated circuit and are respectively connected to them." (Column 1, lines 40-53, in Launay.) Moreover,

according to Launay, his invention "improves the imbedding of the integrated circuit in a board to prevent fraudulent use ... (Column 1, lines 54-58, in Launay.)

Yukawa disclosed a scheme for a semiconductor device having a semiconductor chip bonded on a radiator plate (e.g., 10) via intervening bonding layer (e.g., 12). In accordance with Yukawa's disclosure, the bonding layer comprises a laminated structure including a thermoplastic film bonding layer (e.g., 12a) and a paste-based bonding layer (e.g., 12b). In the semiconductor device according to Yukawa, a uniform bonding layer with a sufficient thickness is provided such that blistering, which causes reduction in the bonding strength as well as reduction in the ability to dissipate heat of the bonding layer, is prevented. (Column 3, lines 17-32, in Yukawa.)

As is evident from the disclosures of Launay and Yukawa, one of ordinary skill would not have been led to combine the teachings therein since their disclosures are directed to totally different objectives. That is, their disclosures, it is submitted, are not combinable. This will become evident with the following showings.

The semiconductor circuit board of Launay, such as in connection with an IC card, contains the following steps:

> Step 1 -- fixing strip 3, having window 23, on support 2 in which antenna 6 is formed; and
> Step 2 -- the semiconductor apparatus is installed into the window 23 (cavity 4);

In accordance with Launay's scheme, strip 3 is formed to protect the antenna that is on support 2. It is submitted, strip 3 does <u>not</u> function as a stress relaxing layer as that called for with regard to the "insulating resin layer" of the present invention. Also, strip 3 and support 2, according to Launay, are made of material formed independently; therefore, the strip 3 in Launay is not formed by printing resin on support 2. With regard to Figs. 4 and 5 in Launay, since the IC circuit (chip) needs

to be connected with the antenna 6, it, therefore, is disposed at an edge other than at the center of the board (see Fig. 1, in Launay.) It is evident, therefore, that Launay neither disclosed nor hinted at the need for providing an insulating layer having a function for relaxing stress occurring between the semiconductor apparatus and the substrate. It is submitted, also, Launay failed to disclose or even hint at forming an insulating layer on the wiring substrate.

Yukawa disclosed using a bonding layer, namely, a two-layer laminate including a thermal plastic film bonding layer 12a and a paste-based bonding layer 12b (see Fig. 1). Clearly, therefore, not only would one of ordinary skill not have been led to combine the teachings of Launay and Yukawa but, moreover, such a combination, it is submitted, is not achievable. For example,

(1) the technical fields of Launay and Yukawa are completely different, applicants submit. One scheme is directed toward an integrated circuit board apparatus such as with regard to an IC card and the other is in connection with a semiconductor apparatus;

(2) both the purpose and the means for solving the problems to which Launay's and Yukawa's disclosures are directed are completely different from that of the present invention;

(3) the function of strip 3 in Launay and the adhering layer 12 in Yukawa are completely different and, also, the disposed positions thereof are also completely different. Therefore, those elements in either Launay or Yukawa could not have been replaced from the teachings of the other; and

(4) the processes associated with the formation of the strip 3 in Launay as well as that of the adhering layer 12 in Yukawa are completely different. It is submitted, therefore, the process of Yukawa could not have been employed in Launay.

Assuming, *arguendo*, that Launay's disclosure was combinable with Yukawa's disclosure, the invention would still not have been realizable therefrom even if combined with the other cited art documents. For one, if strip 3 is formed by resin having a stress relaxing function, then the strip 3 becomes deformed due to thermal stress. As a result of such deformation of strip 3, the antenna that would necessarily be interposed between that strip 3 and board 2, according to Launay, would be destroyed and cut off, thereby preventing Launay from achieving his purpose. Also, since protection resin 18 in Launay, which is used for filling the semiconductor circuit 1 and the window, is necessarily present, the displacement of the integrated circuit by deformation of the strip 3 would lead to a break in the connection of the antenna in the connection terminal.

If a strip such as strip 3 in Launay has a stress relaxing function, which is deformable, it is not a desirable feature when ones intent is to protect the antenna in the support 2. Accordingly, even if one would have attempted to apply Yukawa's disclosure in combination with Launay, it would not have been possible to add a stress relaxation related function to a strip such as strip 3 in Launay, at least for the above stated reasons. Clearly, one would not have been led to combine the teachings of Launay and Yukawa.

With regard to claim 1 of the invention, since the "insulating resin layer" functions as a stress relaxing layer and is of a thick film provided on the substrate of the semiconductor module, the semiconductor module can be installed to another substrate (board) without the need for an underfill. Neither Launay nor Yukawa, each taken separately or, for that matter, combinedly, disclosed at least such featured aspects, according to claim 1. It is noted that other ones of the independent claims also call for a stress relaxing (mollifying) layer.

As to the printing by mask, as called for in claims 3 and 4, for example, neither Launay nor Yukawa even hinted at such featured characteristics as that called for in these claims. Shoji did disclose employing a masking technique. However, Shoji neither disclosed nor suggested forming a thick film insulating layer including a stress relaxation function as that presently called for. Namely, Shoji differed from the present invention at least in connection with the portion for which printing with a mask is being carried out. Moreover, Shoji only disclosed, it is submitted, printing with a mask as a production method. Accordingly, even if one of ordinary skill would have attempted to combine Shoji with Launay and Yukawa, there still would not have been realized therefrom a scheme as that presently called for. Shoji also failed to disclose or suggest a scheme further calling for the formation of a plurality of stress relaxation layers entirely on a substrate composed of a plurality of wiring substrates.

It is noted that the invention according to each of independent claims 15-17 are characterized, also, as not employing an underfill. Generally, the thermal expansion coefficient is different from that of a semiconductor apparatus and a substrate to which the semiconductor apparatus is mounted. Lee disclosed a scheme in which a semiconductor package is sealed by resin sealing the semiconductor chip. As a result, therefore, underfill is not necessary therein.

In accordance with the present invention, by utilizing silicon of which the thermal expansion coefficient thereof is substantially the same as that of the semiconductor apparatus for installing the substrate, a semiconductor module with a highly reliable connection effected between the semiconductor apparatus and the substrate to which it is mounted is achievable, irrespective of whether the semiconductor apparatus is resin sealed or not, without underfill. Also, the invention according to claim 16 calls for a scheme in which the semiconductor device

(semiconductor apparatus) is structured to include an insulating layer (having the function of a stress relaxing layer) of a thick film, without underfill, thereby realizing a semiconductor module of a high connection reliability between that of the semiconductor device (apparatus) and the substrate to which it is mounted on.

Claim 17 calls for a scheme in which a thick film insulating layer that functions as a stress relaxing layer is not only provided in connection with the semiconductor apparatus (semiconductor device) but, also, is provided on the semiconductor module substrate. As a result, therefore, the semiconductor module can be mounted into another substrate such as a wiring substrate without an underfill. It is submitted, the invention, according to the independent claims as now amended as well as according to the corresponding dependent claims thereof, could not have been rendered obvious at least for the reasons noted above.

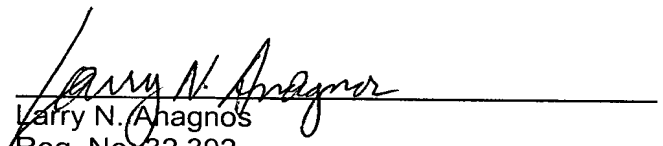
It is noted that none of the other cited references of the outstanding rejections overcame the deficiencies discussed above in connection with Launay and Yukawa. Therefore, even if one of ordinary skill would have applied the teachings of those additional references to Launay and Yukawa in a manner as that cited in the outstanding Office Action, the invention still could not have been achievable, at least for the reasons described hereinabove.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, reconsideration and withdrawal of the outstanding objections/rejections as well as a favorable action therefor on all of the presently pending claims and an early formal Notification of Allowability of the above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the

filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (500.40506X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



Larry N. Anagnos
Reg. No. 32,392

LNA/dks
703-312-6600